AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below:

1. (Currrently Amended) An apparatus, comprising:

- an inductor capacitor (LC) tank;

- a drive circuit including a first generator, coupled to the LC tank, to drive the LC tank, and a current source, coupled to the first generator, to provide a source current to the first generator; [[and]]

- a feedback loop circuit including a peak detect circuit, coupled to the LC tank, to generate a peak detect voltage signal representing an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source, to compare the peak detect voltage signal and the single reference voltage signal and to generate an analog bias signal in response to a difference between the peak detect voltage signal and the single reference voltage, with the currrent source being adapted to adjust a magnitude of the source current in response to the analog bias signal;

- the LC tank further including a first tank terminal and a second tank terminal;

- the first generator including a negative resistance generator having a first and a second drive transistor coupled to the first and second tank terminals; the first and second drive transistors having a pair of commonly coupled terminals;

- the current source including a single current source transistor coupled to the commonly coupled terminals to provide the source current to the first and second drive transistors;

- the peak detect circuit including a first detect transistor coupled to the first tank terminal; a second detect transistor coupled to the second tank terminal and the first detect transistor; and a detect current source commonly coupled to the first and second detect transistors;

- the reference voltage circuit including a first reference transistor operable to receive a reference bias signal; a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal; and a reference current source commonly coupled to the first and second reference transistors; and

- the first detect and first reference transistors being identical in design; the second detect and second reference transistors being identical in design; and the detect and reference current sources being identical in design.

2. (Original) The apparatus according to claim 1, wherein a capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

3. (Original) The apparatus according to claim 2, wherein the LC tank further comprises a first tank terminal and a second tank terminal; the first generator comprises a negative resistance generator including a first and a second drive transistor coupled to the first and second tank terminals; the first and second drive transistors have a pair of commonly coupled terminals; the current source is a single current source transistor coupled to the commonly coupled terminals to provide the source current to the first and second drive transistors; and the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.

4. (Canceled)

5. (Canceled)

6. (Currently Amended) The apparatus according to claim [[5]]1, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first

detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

7. (Original) The apparatus according to claim 6, wherein the LC tank has a first and a second LC resonator, the first LC resonator including a first inductance coupled between a supply voltage and the first tank terminal and a first variable capacitor coupled between the first tank terminal and a control node, the second LC resonator including a second inductance coupled between the supply voltage and the second tank terminal and a second variable capacitor coupled between the second tank terminal and the control node, the first drive transistor being coupled to the first tank terminal and cross-coupled the second tank terminal and the second drive transistor being coupled the second tank terminal and cross-coupled to the first tank terminal.

8. (Original) The apparatus according to claim 7, wherein the first drive transistor, the second drive transistor, and the current source transistor are MOSFETS; a drain of the first drive transistor is coupled to the first tank terminal; a gate of the first drive transistor is cross-coupled to the drain of the second tank terminal; a drain of the second drive transistor is coupled the second tank terminal; a gate of the second transistor is cross-coupled to the first tank terminal; a source of the first drive transistor and a source of the second drive transistor are commonly coupled to a drain of the current source transistor; a source of the current source transistor is coupled to ground; and a gate of the current source transistor is coupled to the output terminal of the operational amplifier to receive the analog bias signal.

9. (Original) The apparatus according to claim 8, wherein the operational amplifier is a folded cascode operational amplifier.

10. (Currently Amended) An apparatus, comprising:

- an inductor capacitor (LC) tank having a pair of tank terminals;

- a drive circuit including a first and a second drive transistor, coupled to the pair of tank terminals and having a pair of commonly coupled terminals, and a single current source transistor, connected to the commonly coupled terminals, to provide a source current to the first and second drive transistors;

- a feedback loop circuit including a peak detect circuit, with a pair of input terminals coupled to the pair of tank terminals, to generate a peak detect voltage signal representative of an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source transistor, to compare the peak detect voltage signal and the single reference voltage and to generate an analog bias signal in response to a difference between the peak detect voltage signal and the single reference voltage, with the current source transistor being adapted to adjust a magnitude of the source current in response to the analog bias signal;

- the peak detect circuit including a first detect transistor coupled to the first tank terminal; a second detect transistor coupled to the second tank terminal and the first detect transistor; and a detect current source commonly coupled to the first and second detect transistors;

- the reference voltage circuit including a first reference transistor operable to receive a reference bias signal; a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal; and a reference current source commonly coupled to the first and second reference transistors; and

- the first detect and first reference transistors being identical in design; the second detect and second reference transistors being identical in design; and the detect and reference current sources being identical in design.

11. (Original) The apparatus according to claim 10, wherein a compensation capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

12. (Original) The apparatus according to claim 10, wherein the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.

13. (Canceled)

14. (Canceled)

15. (Currently Amended) The apparatus according to claim [[14]]10, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

16. (Original) The apparatus according to claim 12, wherein the LC tank has a first and a second LC resonator, the first LC resonator including a first inductance coupled between a supply voltage and the first tank terminal and a first variable capacitor coupled between the first tank terminal and a control node, the second LC resonator including a second inductance coupled between the supply voltage and the second tank terminal and a second variable capacitor coupled between the second tank terminal and the control node, the first drive transistor being coupled to the first tank terminal and cross-coupled the second tank terminal and the second drive transistor being coupled the second tank terminal and cross-coupled to the first tank terminal.

17. (Original) The apparatus according to claim 16, wherein the first drive transistor, the second drive transistor, and the current source transistor are MOSFETS; a drain of the first drive transistor is coupled to the first tank terminal; a gate of the first drive transistor is cross-coupled to the drain of the second tank terminal; a drain of the second drive transistor is coupled the second tank terminal; a gate of the second transistor is cross-coupled to the first tank terminal; a source of the first drive transistor and a source of the second drive transistor are commonly coupled to a drain of the current source transistor; a source of the current source transistor is coupled to ground; and a gate of the current source transistor is coupled to the output terminal of the operational amplifier to receive the analog bias signal.

18. (Original) The apparatus according to claim 12, wherein the operational amplifier is a folded cascode operational amplifier.

19. (Currently Amended) A system, comprising an integrated circuit having a receiver, the receiver having a phase lock loop (PLL) to recover a clock signal from a data signal; the PLL including a phase detector with a first input to receive the data signal; a loop filter having an input coupled to the output of the phase detector; and a voltage controlled oscillator (VCO) having an input coupled to the output of the loop filter and an

output coupled to a second input of the phase detector; the VCO including an inductor capacitor (LC) tank; a drive circuit including a first generator, coupled to the LC tank, to drive the LC tank and a current source, coupled to the first generator, to provide a source current to the first generator; and a feedback loop circuit including a peak detect circuit, with a pair of input terminals coupled to the LC tank, to generate a peak detect voltage signal representing an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source, to compare the peak detect voltage signal and the single reference voltage and to generate an analog bias signal in response to a difference between the peak detect voltage signal and the single reference voltage, with the current source being adapted to adjust thea magnitude of the source current in response to the analog bias signal; the LC tank having a first tank terminal and a second tank terminal; the first generator including a negative resistance generator having a first and a second drive transistor coupled to the first and second tank terminals; the first and second drive transistors having a pair of commonly coupled terminals; the current source comprising a single current source transistor coupled to the commonly coupled terminals to provide the source current to the first and second drive transistors; the peak detect circuit including a first detect transistor coupled to the first tank terminal; a second detect transistor coupled to the second tank terminal and the first detect transistor; and a detect current source commonly coupled to the first and second detect transistors; the reference voltage circuit including a first reference transistor operable to receive a reference bias signal; a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal; and a reference current source commonly coupled to the first and second reference transistors; the first detect and first reference transistors being identical in design; the second detect and second reference transistors being identical in design; and the detect and reference current sources being identical in design.

20. (Original) The system of claim 19, further comprising a fiber-optical data communications channel, coupled to the receiver, to provide the data signal to the receiver.

21. (Original) The system according to claim 19, wherein a capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Currently Amended) The system according to claim [[24]]19, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Previously Presented) The apparatus according to claim 5, wherein a capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

30. (Previously Presented) The apparatus according to claim 29, wherein the pair of input terminals of the peak detect circuit are coupled to the first and the second tank terminals through a first and a second blocking capacitor.

31. (Previously Presented) The apparatus according to claim 14, wherein the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.